

UNIVERSAL MODULATOR/DEMODULATOR

Field of the Invention

The present invention relates to the field of electronic circuits and, more particularly, to modulation/demodulation devices for modulating a high-frequency electrical signal. Such devices may be for sending information via modulated electronic signals to a remote device and demodulating the modulated electrical signals to extract the information therefrom. More specifically, the present invention relates to modulation/demodulation devices which are used in the field of home automation, or in the area of energy metering for remotely metering electricity meters, modifying electricity billing rates, commanding the on/off switching of household appliances, etc.

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Background of the Invention

There are many high frequency electrical signal modulation techniques used in the field of home automation and energy metering, such as amplitude modulation (AM), spread frequency shift keying (SFSK), and frequency shift keying (FSK). Information may be

- encoded according to different protocols which determine the format of the messages to be sent, where each message includes binary signals which control the modulator at the sending end. Upon reception, the
- 5 demodulator detects the high frequency modulated signals and extracts the binary information of the message sent. The extracted binary signals are then interpreted by an appropriate device, such as a microprocessor, depending on the protocol.
- 10 Because the appliances of a home automation system may receive and send messages, they are generally equipped with a modulation/demodulation device. Yet, appliances of a home automation system are typically adapted to operate according to one type
- 15 of modulation. As a result, they cannot be used in another home automation system that implements another type of modulation.

Summary of the Invention

In view of the foregoing, an object of the

20 invention is to provide a modulation/demodulation device which can function with different types of modulation.

This and other objects, features, and advantages in accordance with the present invention are

25 provided by a modulation/demodulation device capable of operating according to a plurality of types of modulation using different carrier frequencies. The modulation/demodulation device may include a modulator for modulating, according to the type of modulation, at

least one signal at a carrier frequency by a signal of a determined duration and representative of binary information supplied by a microprocessor. The modulated signal may be applied to a sending/receiving
5 device for sending to a remote site.

A demodulator may also be included for receiving modulated signals from a remote site via the sending/receiving device and demodulating the modulated signals. More specifically, the demodulating may be
10 done by determining the type of modulation used for the received signals and their carrier frequency/frequencies, supplying signals from an analysis of the signals received according to the determined type of modulation, and detecting the
15 signals of determined duration representative of binary information to make them accessible by the microprocessor.

Brief Description of the Drawings

20 Other advantages and characteristics of the present invention will become more apparent from the following description of the preferred embodiments in conjunction with the appended drawings, in which:

FIG. 1 is a schematic block diagram of a
25 modulation/demodulation device in accordance with the invention that is connected at one end to a message encoding/decoding microprocessor and at the other end to a modulated electrical signal sending/receiving device;

FIG. 2 is a more detailed schematic block diagram of the modulator of the modulation/demodulation device of FIG. 1;

5 FIG. 3 is a more detailed schematic block diagram of a first part of the demodulator of FIG. 1;

FIG. 4 is a diagram of a received signal selection device according to the invention;

FIG. 5 is a schematic block diagram of the signal analyzing circuit of FIG. 1; and

10 FIGS. 6a, 6b, and 6c are signal diagrams illustrating operation of the circuit of FIG. 5.

Detailed Description of the Preferred Embodiments

The invention will be described herein within the context of an application with existing types of 15 modulation and protocols. By way of example, these may include: EURIDIS, operating in amplitude modulation with a 50kHz carrier frequency (MA mode or signal); Power Line Area Network (P.LAN), operating in frequency modulation between 60 kHz and 90 kHz in the field of 20 meter reading (MB mode or signal); European Home System (EHS), operating in frequency modulation between 60 kHz and 90 kHz in the field of meter reading (MB mode or signal); EHS, analogous to the above, but operating at 132.5 kHz in the field of automatic controls in 25 domestic automation (MC mode or signal); and Ripple Remote Control (RRC), operating in amplitude modulation at a 175 kHz carrier frequency (MD mode or signal). Of course, the invention is also applicable to other modulation modes, such as amplitude modulation,

frequency modulation, frequency multiplex modulation, and frequency hopping in the field of data encryption (secured transmission).

The modulation/demodulation device 10, or
5 more succinctly modulator/demodulator 10,
illustratively includes a modulator 12 which modulates
a signal at a carrier frequency using a modulation mode
chosen to produce modulated signals. These modulated
signals are applied to a sending/receiving device 14 by
10 which they are sent to a remote site. Further, a
demodulator 16 receives the modulated signals from the
remote site via the sending/receiving device 14.

The demodulator 16 essentially includes a set
of bandpass filters 18, each centered on the carrier
15 frequencies of the modulated signals, and to which are
applied the signals received and detected by the
sending/receiving device 14. The demodulator 16 also
illustratively includes a set of operational amplifiers
20, one per bandpass filter. Each operational
20 amplifier is gain controlled by a gain control circuit.
Additionally, the demodulator 16 illustratively
includes a set of voltage comparators 22, one per
bandpass filter, to detect the modulated signals which
are outside a determined threshold (FIG. 4), and an
25 encoding circuit 24 whose output code identifies the
received signal MA, MB, MC or MD. The demodulator 16
also includes a demultiplexing circuit 26 for acting on
the received signals and selecting the signal that is
to be demodulated among the received signals MA, MB, MC
30 or MD, and an analyzer circuit 28 acting on the

selected signal MA, MB, MC or MD to extract the data contained in the modulated signal.

In a sending mode, the data to be sent are supplied to a modulator 12 by a microprocessor 30, 5 which also indicates the type of modulation that will apply. In a receiving mode, the data extracted from the received modulated signal are supplied to the microprocessor 30, and the signal is decoded as a function of the received signal MA, MB, MC or MD and 10 the sending protocol.

The microprocessor 30 provides all the circuits of the modulator/demodulator according to the invention with a clock signal CLK, e.g., pulses at 8 MHz frequency. This clock signal CLK is used by the 15 modulator 12 to produce the modulated signals, and it is also used by the demodulator's analyzer circuit 28 to extract the data in the modulated signals.

The modulator 12 (FIG. 2) generates a sinusoidal signal corresponding to each carrier 20 frequency. The duration of the signals at each carrier frequency are determined by the number of sinusoids at the carrier frequency. To generate this sinusoidal signal at the carrier frequency, the modulator uses a memory 40 which stores the codes representative of the 25 values of the samples of a sinusoidal signal. It is the readout speed of this memory 40 that determines the frequency of sinusoidal signal that will be obtained. The number of samples per sinusoid is equal to R.

To this end, in the FSK mode at a speed of 30 1200 baud, a binary digit 1 is, for example,

- represented by a signal at a frequency $F_1 = 71.4$ kHz, while a binary digit 0 is represented by a signal at a frequency $F = 72.6$ kHz with a central frequency of 72 kHz and a mean period of 13.88 microseconds. Also, a
- 5 speed of 1200 baud corresponds to a period of 833 microseconds, i.e., around 60 periods at the 72 kHz frequency. In the case where a bit occupies half the period at most, its maximum duration will be 30 periods of the 72 kHz signal.
- 10 The modulator 12 in accordance with the invention illustratively includes the memory 40, which is of the read-only (ROM) type. The number of samples per sinusoid may be 25, for example, with a readout frequency of 1.815 MHz for the frequency $F_0 = 72.6$ kHz.
- 15 Further, the modulator 12 also includes two counters 42 (or CPT1) and 44 (or CPT0) which scan the addresses of the memory 40 to read the codes representative of the samples of each sinusoid. A multiplexing circuit 46 selects either the addresses supplied by the counter
- 20 CPT1, or those supplied by the counter CPT0, and a control circuit 48 operates on the multiplexing circuit as a function of a binary digit 1 or 0 to be sent.
- Additionally, a counter circuit 50 totals the number N of pulses at frequency F_1 and the number M of
- 25 pulses at the frequency F_0 . This count is in fact carried out by a countdown using two countdown counters, one 50_{F_1} for the number N and the other 50_{F_0} for the number M, the numbers N and M being loaded by the microprocessor 30. The modulator 12 also
- 30 illustratively includes a clock circuit 52 which

supplies the counting pulses of counters 42 and 44 to obtain the frequencies F1 or F0, i.e., the rate of reading the code representative of the samples, and a programming circuit 54 for the clock circuit 52, which
5 is loaded by the microprocessor 30 as a function of frequencies F1 and F0. The modulator 12 may further include a selection circuit 56 which selects the type of modulation (e.g., AM, FSK or SFSK) a digital-to-analog converter 58 for converting the codes supplied
10 by the memory 40, a bandpass filter 60 for eliminating the signals at unwanted frequencies, and an operational amplifier 62 for amplifying the modulated signals and applying them to the sending/receiving device 14.

The operation of the modulator illustrated in
15 FIG. 2 is then as follows. For a given type of modulated signal to be obtained, the microprocessor 30 loads the programming circuit 54, the countdown counters 50_{F_1} and 50_{F_0} , and the modulation selection circuit 56 with the numbers N and M. The clock circuit
20 52 supplies the counting pulses of counters the CPT1 and CPT0 to obtain the high-frequency sinusoidal signals F1 and F0. The choice between the addresses supplied by counter CPT1 or by counter CPT0 is made by the multiplexing circuit 46 as a function of the binary
25 digit to be sent, which is supplied by the control circuit 48.

The number N of sinusoids at frequency F1 for a binary digit 1 is counted down by the countdown counter 50_{F_1} , while the number M of sinusoids at
30 frequency F0 for a binary digit 0 is counted down by

the countdown counter 50_{F_0} . Each countdown counter is decremented by 1 every time the corresponding counter CPT1 or CPT0 has gone through a complete cycle. As already explained with reference to FIG. 1, the signals
5 supplied by the receiver of the sending/receiving device 14 are applied to a set of bandpass filters 18. Each of the bandpass filters 18 filters a given frequency band which corresponds to that of the modulated signal that may hypothetically be received.

10 Each outgoing signal V_{in} from a bandpass filter of the set 18 is applied to an operational amplifier 80 whose gain is controlled by a resistive network 82 formed by switchable resistors to modify the feedback, and hence the gain, of the operational
15 amplifier 80. The resistors of the network are switched by an up/down counter 84 whose current value varies as a function of the amplitude of the signal V_{IN} relative to three reference thresholds, namely $V_{refnominal}$, $V_{refmaxi}$ and $V_{refmini}$. To this end, the
20 output terminal of the operational amplifier 80, which supplies an amplified signal V_{IN} , is connected to one of two input terminals of three comparators 86, 88 and 90. The other input terminal is connected to voltage sources 96, 98 and 100 which respectively supply the
25 reference threshold values $V_{refnominal}$, $V_{refmini}$ and $V_{refmaxi}$.

The output terminals of comparators 86, 88 and 90 are connected to a logic device 92 which performs several functions. One of these functions is
30 decreasing the value of the up/down counter 84 when V_{IN}

is greater than Vrefmaxi to reduce the gain. Further, the logic device 92 increases the value of the up/down counter 84 when VIN is greater than Vrefmini but less than Vrefnominal to increase the gain. Another 5 function of the logic device 92 is not to change the value of the up/down counter when VIN is greater than Vrefnominal but less than Vrefmax, and thus not to modify the gain.

The logic device 92 includes AND gates 94, 10 102 to 112, inverters 114 to 120, and an OR gate 122. The AND gate 94 includes three input terminals which are connected respectively to the output terminal of comparator 86, the output terminal of comparator 88, and the output terminal of comparator 90 via the 15 inverter 118. The output terminal of the AND gate 94 is connected to one of two input terminals of the AND gate 102 via the inverter 114. The other input terminal of the AND gate 102 is connected to a terminal 124 which supplies a clock signal at a suitable 20 frequency.

The output terminal of the AND gate 102 is connected to one of two input terminals of the AND gate 106, the other input terminal of which is connected to the output terminal of comparator 90. This output 25 terminal of the comparator 90 is also connected to one of two input terminals of the AND gate 112, the other input terminal of which is connected both to the output terminal of the AND gate 106 and to one of two input terminals of the OR gate 122. The other input terminal

of the OR gate 122 is connected to the output terminal of the AND gate 108.

The AND gate 108 has three input terminals which are connected respectively to the clock terminal 5 124, the output terminal of comparator 88, and the output terminal of comparator 86 via the inverter 120. The output terminal of the inverter 120 is also connected to one of three input terminals of the AND 10 gate 110, and to one of two input terminals of the AND gate 104. The output terminal of the AND gate 110 is connected to the count input terminal 126 of the up/down counter 84, while the output terminal of the AND gate 112 is connected to the count-down input 128 of the up/down counter 84. The second input terminal 15 of the AND gate 104 is connected to the output terminal of the comparator 88 via an inverter 116, and the output terminal is connected to a terminal 130 indicating that the received signal has an amplitude VIN which is less than Vrefmini.

20 The operation of the device illustrated in FIG. 3 is as follows. For the case where VIN is greater than Vrefnominal and Vrefmini but less than Vrefmaxi, the output terminals of comparators 86, 88 and 90 are respectively at logic states 1, 1 and 0. 25 Also, by logic combinations, AND gates 110 and 112 are blocked so that the up/down counter 84 does not change its count value.

For the case where VIN is less than Vrefnominal but greater than Vrefmini, the output 30 terminals of comparators 86, 88 and 90 are respectively

at logic states 0, 1 and 0. Further, by logic combinations, AND gate 110 is open and allows the clock pulses supplied by terminal 124 to pass through. These pulses are then applied to the count input 126 of the
5 up/down counter 84 whose value increments and causes a gain increase in amplifier 80 via the resistor network 82.

For the case where VIN is greater than Vrefnominal, Vrefmini, and Vrefmaxi, the output
10 terminals of comparators 86, 88 and 90 are all at a logic state 1 and, by logic combination, the AND gate 112 is open to allow the clock pulses supplied by clock terminal 124 to pass through. These pulses are applied to the countdown input 128 of the up/down counter 84
15 whose value decrements and causes a gain reduction in amplifier 80 via the resistor network 82.

For the case where VIN is less than Vrefnominal, Vrefmini, and Vrefmaxi, the output terminals of comparators 86, 88 and 90 are all at a
20 logic state 0 and, by logic combination, the output terminal of the AND gate 104 is at logic state 1. Thus, a signal is produced on the output terminal 130 which is interpreted as a received signal that is not correct.

25 The signal VIN of each receiving channel MA, MB, MC and MD is filtered (18), amplified (20), and then applied to a demultiplexing circuit 26 and a received channel detector circuit 140 whose output signal controls the multiplexing circuit 26. The
30 detector circuit 140 includes four comparators 142_{MA},

142_{MB}, 142_{MC} and 142_{MD}, and an encoding circuit 144 for encoding output logic states of the comparators 142. In each comparator, the signal VIN corresponding to the signal received on the channel is compared to a
5 threshold VrefMA, VrefMB, VrefMC and VrefMD.

If one of the signals VIN exceeds the threshold, the output terminal of the corresponding comparator passes to a logic state 1, whereas the output terminals of the other comparators remain at a
10 logic state 0. These logic states 1 and 0 are encoded in the encoding circuit 144 which supplies a two-digit code applied to the demultiplexing circuit 26 to select the channel having produced a logic state 1 at the output of one of the comparators 142. This code is
15 also applied to the microprocessor 30 to indicate to the latter the identity MA, MB, MC or MD of the received channel.

A diagram illustrating in greater detail the analyzer circuit 28 of FIG. 1 may be seen in FIG. 5.
20 The analyzer circuit 28 receives, via the demultiplexing circuit 26, the output signal VIN from one of the operational amplifiers 20. The amplifier input signal is designated Vin. The demodulation circuit 28 is based on the measurement of the number N
25 or M of sinusoids of the carrier frequency F1 or F0 in the binary digit or bit 1 or 0. The numbers N and M are given by the microprocessor 30, the latter knowing the channel MA, MB, MC or MD currently received. It also indicates the value of the frequency of the clock
30 signals to be used.

As shown in FIG. 5, the demodulator circuit includes a clock circuit 220 which supplies a pulse signal whose frequency is determined as a function of the channel MA, MB, MC or MD being received. This

5 clock circuit includes a program register 260 which is loaded by the microprocessor 30 and produces the different clock signals. For example, these clock signals may be provided to a circuit 262 to obtain the sampling CLK signal and to a counter 258 which is

10 loaded by the microprocessor 30 with the number of bits of the frame to be received. A translator circuit 200 translates the signal VIN so that it evolves on either side of the zero value, and a sample-and-hold circuit 202 samples the signal VIN. The sample-and-hold

15 circuit 202 is controlled by the clock signal CLK supplied by circuit 220.

Furthermore, an analog-to-digital converter 204 encodes the samples supplied by the sample-and-hold circuit 202, and a digital comparator 206 compares,

20 sample code by sample code, the code representative of the amplitude to a code representing a reference voltage Vrefn. A zero crossing detector 212 is also included for the signal VIN and includes two flip-flops 208 and 210. These allow the detection of the half-

25 period and period of the signal at the carrier frequency F1 and/or F0. A validation circuit 230 is for validating the period of the sinusoid of the signal at the carrier frequency by counting the number of samples, and a detector circuit 240 detects logic state

30 1 or 0 bits by counting the number N or M of sinusoids.

The zero crossing detector 212 includes two D-type latches 208 and 210. The D input terminal of the latch 208 is connected to the output terminal of the digital comparator 206 and to the D input terminal 5 of the latch 210. The clock input of the latch 208 receives the clock signal corresponding to the sampling frequency such that it changes state at the leading edge of that pulse if the D input terminal changes state. The Q1 output terminal of the latch 208 is 10 connected to one of two input terminals of an AND gate 212, the other input terminal of which receives the sampling clock signal CLK. The other output terminal $\overline{Q1}$ of the latch 208 is connected to the clock input terminal of the latch 210. The output terminal Q2 of 15 the latch 210 is connected to an input terminal of a counter 214 which counts the samples designated as "bad", i.e., those which do not correspond to a half sinusoid of the carrier frequency signal.

The second output terminal $\overline{Q2}$ which 20 corresponds to a period of the carrier signal designated as "good," is connected to one of two input terminals of an AND gate 216 of the validation circuit 230. The validation circuit 230 includes a "bad" sample counter 214, and a "good" sample counter 218 25 whose input terminal is connected to the output terminal of AND gate 212. Further, a digital comparator 222 effects a comparison between the contents of the counter 218 and the number N of samples expected per sinusoid of the signal at the carrier 30 frequency. Again, the number N is supplied by the

microprocessor 30. Additionally, the AND gate 216 receives at its second input terminal the signal at logic state 1 resulting from a positive (matching) comparison. It produces at its output terminal a 5 validation signal validating the period of the signal at the received carrier frequency that is applied to the detector circuit 240.

The detector circuit 240 includes a counter 242 for the number P of periods of the carrier signal, 10 whether that number corresponds to a logic state 1 bit or a logic state 0 bit. Also, a first digital comparator 244 compares the number P to the number N of periods corresponding to the channel being received for a logic state 1 bit, where number N is given by the 15 microprocessor 30 and recorded in a register 246. A second digital comparator 248 compares the number P to the number M of periods corresponding to the channel being received for a bit at logic state 0, this number M being given by the microprocessor 30 and recorded in 20 a register 250.

Furthermore, an OR gate 252 is included and one of its two input terminals receives the logic state 1 bit of the comparator 244. Its other input terminal receives the logic state 0 bit of the comparator 248. 25 A shift register 256 stores the logic state 1 and 0 bit signals detected by comparators 244 and 248 via the OR gate 252, and a shift register 254 also stores the logic 1 and 0 bit signals detected by comparators 244 and 248. It also receives the signal from the output 30 Q2 of latch 210 indicating whether or not bad samples

are received for the bit currently analyzed. It is the contents of the registers 254, 256 that are transferred to the microprocessor 30 to be analyzed in accordance with the communications protocol and, in the first 5 place, to implement an error correction code taking into account the state of Q2.

The operation of the demodulation circuit according to the diagram of FIG. 5 is as follows. The signal VIN, after translation and shaping in circuit 10 200, takes the form of the envelope 300 shown in the diagram of FIG. 6a. It is sampled in circuit 202 to obtain samples 302 in synchronization with the clock pulses CLK (FIG. 6b). The amplitude of each sample is encoded, and the corresponding code is compared in 15 comparator 206 with a code that represents a reference voltage Vref.

The latch 208 is in the logic state 1 while $VIN > V_{ref}$, as shown in the diagram of FIG. 6c which illustrates the signal at the output terminal Q1 (304_1 , 20 304_2 , 304_3 and 304_4). The intervals between signals 304_1 to 304_4 represent time periods during which $VIN \leq V_{ref}$. When latch 208 is at logic state 1, the AND gate 212 is open and allows the passage of CLK pulses which are counted by counter 218. When the AND gate 212 is 25 closed, the contents of counter 218 are compared in comparator 222 with the number P expected, it being known which channel is currently being received.

In the case where the signals are equal, the AND gate 216 is open so that the counter 242 is 30 incremented by one unit to indicate that a sinusoid of

the signal at the carrier frequency has been detected.

This counter 242 is incremented by one unit each time a sinusoid of the signal at the carrier frequency is detected. Its content is compared to the value N

5 indicating the presence of a bit at logic state 1 and to the value M indicating the presence of a bit at logic state 0 in respective comparators 244 and 248.

Again, the values of N and M are supplied by the microprocessor 30 with knowledge of the channel

10 currently being received. This comparison is carried out in the presence of a signal coming from the counter 258 and which indicates the position of the bit in the frame currently being received.

If the number of sinusoids is equal to N,
15 then the bit is at logic state 1, while the bit is at logic state 0 if the number of sinusoids is equal to M. The bits 1 and 0 thus detected are stored in the shift register 254 for sending to the microprocessor 30. Provisions are made so that the comparisons performed
20 allow a certain tolerance in the values of N and M.

The invention has been described as using several bandpass filters and several operational amplifiers. However, it is possible to use just one filter and just one operational amplifier using
25 switched capacitor devices which allow a change in the operating frequency. Additionally, the operational amplifier can be connected between the multiplexer 26 and the device 28.